INVESTIGATION OF THE DYNAMIC RANGE PROBLEM

AND PROVIDING SOFTWARE SUPPORT

FOR THE AOL SYSTEM

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FINAL REPORT

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In May 1977, Hampton Institute was awarded a research grant for the "Investigation of the Dynamic Range Problem and Providing Hardware Support for the Airborne Oceanographic Lidar System".

The major objectives of the investigation were as follows:

1. Laser Lidar Dynamic Range Problem: Continued research into the AOL dynamic range was necessary for the successful operation of the System. Past research at Hampton Institute was directed towards the gating of the photomultiplier tube. There is a theoretical limit to the speed to which the photomultiplier tube gain can be changed. This gain change problem is so universal and extremely important that Hampton Institute would like to further investigate this problem. Other possible areas to be investigated would include:

   (a) Logarithmic Amplifiers

   (b) Gain reduction in the first several samples and hold gates of the AOL system.

   (c) High speed light-gating ahead of the photomultiplier tube.

2. General Support: The Digital Systems Laboratory at Hampton Institute was to provide any reasonable assistance to NASA/Wallops Station as may be required during the contract year.

3. Systems Hardware: The Digital Systems Laboratory at Hampton Institute has available personnel with expertise in all facets of computer hardware. These individuals were available to review current hardware, possible required hardware additions, hardware maintenance, guidelines and procedures, and to study the complete system for possible hardware limitations based on changing schedules and priorities.

4. Data Analysis: Methods and procedures were to be established for retrieving information out of the digital data scan, possibly using digital filtering, slope selection, or peak selection. To date all data analysis in the AOL System has used the peak selection method of solution. With the

possibility of using other methods of gating the photomultiplier tube, a thorough investigation will be necessary to determine the possibility of using the other data reduction methods.

During the course of system checkout on the NASA Airborne Oceanographic Lidar System, it has become apparent that the present scheme for providing the system timing is not completely satisfactory. Forty pulses are generated to energize the forty gates leading to the charge digitizers. The present system uses analog gates and delay lines. The gates are susceptible to temperature and voltage variations and the delay lines can promote timing differences if different lengths of cable are used, or if the connectors exhibit different impedance characteristics.

Hampton Institute has investigated the possibility of using a "digital" approach for generating these forty pulses. The solution in terms of general analog and digital circuitry is very straight forward. A general solution is shown in Figure 1.

The general flow of this circuit is that the crystal oscillator provides a stable frequency source. This frequency is then used as a clock to the ring counter. The ring counter is used to propagate a pulse from stage one to stage forty. Each of the outputs have an amplifier for isolation.

This design is very straight forward and easy to implement in the frequency range up to 50 MHZ.

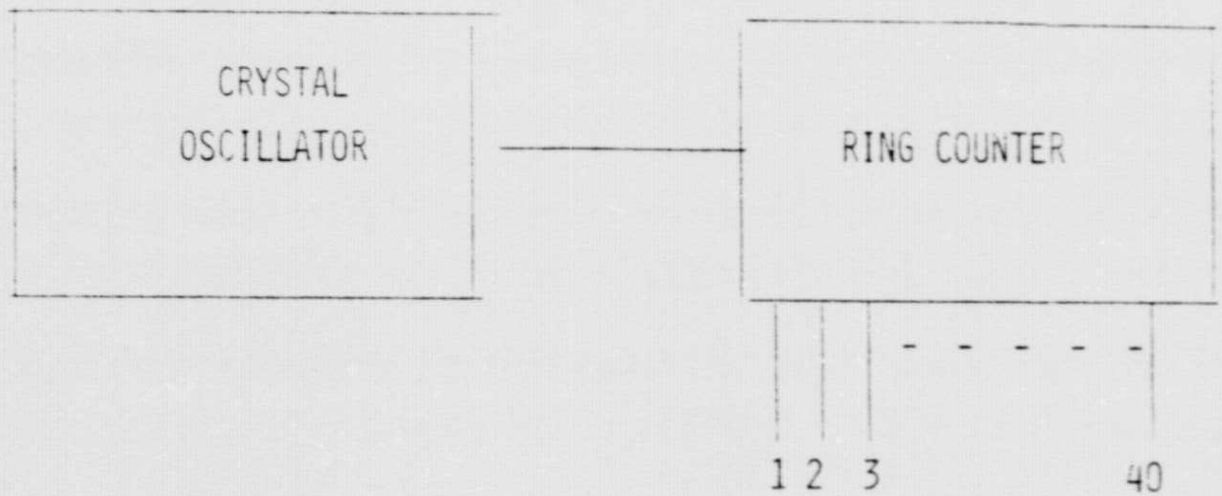


FIGURE 1

For the AOL System a gate pulse width of from about 2 to 6 ns is needed. This dictates an input clock frequency to the shift register of from 100 MHA to 500 MHA. In this range of operation, generating these pulses becomes more of a problem.

Following is a description of the problems associated with each area:

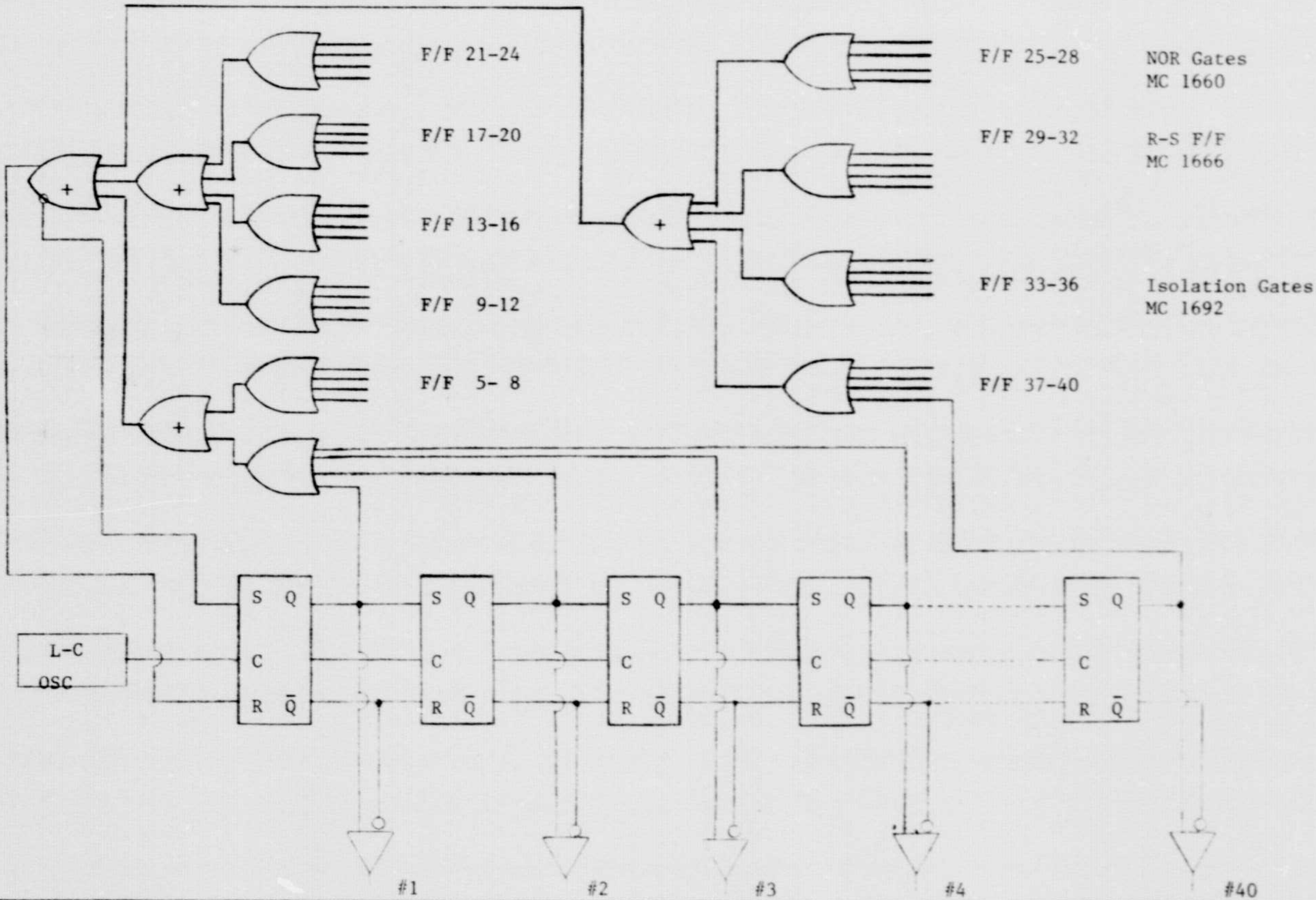
Crystal Oscillator - Crystal Oscillators may be obtained in this frequency with the required output levels. But, presently the optimum AOL pulse width has not been determined.

Ring Counter - The limitation on the ring counter is bandwidth. Presently the fastest available flip-flop that could be used in a ring counter design are limited to 300 MHZ.

As an alternate solution the circuit in Figure 2 is suggested. The crystal oscillator is replaced by a LC oscillator that may be purchased from Hope Electronics. An oscillator with a center frequency of 250 MHZ, adjustable by $\pm$ 25% is selected. This will give a pulse width of approximately 3.3 to 5ns. Since the present pulse width is 4ns, this adjustment range will give some latitude in selecting the best pulse width.

The ring counter and associated feedback logic is made up of MECL III, (or equivalent) emitter coupled logic. The flip-flops are MC 1666, the NOR gates MC 1660, and the isolation gates MC 1692.

Figure 2



F/F 21-24
F/F 17-20
F/F 13-16
F/F 9-12
F/F 5- 8
F/F 25-28
F/F 29-32
F/F 33-36
F/F 37-40
NOR Gates
MC 1660
R-S F/F
MC 1666
Isolation Gates
MC 1692
L-C
OSC
S
Q
C
R
Q̄
#1
#2
#3
#4
#40

In regard to use of a high speed ring counter to develop 40 gating pulses for the NASA Wallops LIDAR systems, Hampton Institute (HI) procurred a small quantity of MECL III high speed oogic.

A test circuit was made (Figure 2) and measurements taken. Test equipment was a Techtronix 475 oscilloscope, Techtronix PG501 pulse generator and HP 6215A power supplies. As can be noted from the test equipment list, the MECL III logic is specified to perform past the limits of the test equipment. An examination of the waveforms on Fig. 1 shows that the logic does perform as best as it can be exercised by the available equipment.

While care was taken on the breadboard, it is obvious from the noise on -5.2VDC and GND that a more sophisticated laboratory test facility is required. HI at this point does not have such a facility.

HI also made an effort to obtain a high speed L-C oscillator. Despite an official purchase order and several calls to the manufacturer, no such device was delivered.

It should be noted that the required gating pulse for Wallops is in the order of 3ns and goes from 0 to -.5VDC. Should the MECL III logic prove feasible for a ring counter, some sort of level changer is required as the MECL III level is from -.5VDC to -2.0VDC. Perhaps a high speed transistor such as a 2N5841 could be used for this purpose.

Figure 3

TEST CIRCUIT

All Logic MECL III